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Your reference	PHGB030213GBP
Patent application number *(The Patent Office will fill in this part)*	0327793.6 ✓
	01DEC03 E836115-4 D02879 P01/7700 0.00-0327793.6
Full name, address and postcode of the or of each applicant (*underline all surnames*)	KONINKLIJKE PHILIPS ELECTRONICS N.V. GROENEWOUDSEWEG 1 5621 BA EINDHOVEN THE NETHERLANDS
Patents ADP Number (*if you know it*)	07419294001 ✓
If the applicant is a corporate body, give the country/state of its incorporation	THE NETHERLANDS
Title of the invention	TRENCH MOSFET
Name of your agent (*if you have one*)	
"Address for service" in the United Kingdom to which all correspondence should be sent (*including the postcode*)	Philips Intellectual Property & Standards Cross Oak Lane Redhill Surrey RH1 5HA
Patents ADP number (*if you know it*)	08359655001 ✓

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Description	7
Claims(s)	2
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11. I/We request the grant of a patent on the basis of this application.

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DESCRIPTION

TRENCH MOSFET

The invention relates to a trench MOSFET (metal oxide semiconductor field effect transistor), and particularly but not exclusively to a trench MOSFET structure suitable for use as control and sync FETs.

Low-voltage trench MOSFETs are commonly used, for example in voltage regulator modules (VRMs) in power supplies for electronic equipment such as personal computers. Commonly, a pair of MOSFETs are used, known as a control FET and a Sync FET. The ideal characteristics of these FETs differ slightly. For the Sync FET the conduction power loss should be as low as possible. Since the conduction power loss is proportional to the specific on-resistance ($R_{ds,on}$) this parameter should be reduced. For the control FET on the other hand the switching loss should be minimised, which is proportional to the gate-drain charge density (Q_{gd}).

A figure of merit (FOM) has been defined as the multiple of $R_{ds,on}$ and Q_{gd} to provide an indication of how suitable a transistor is in for use in VRMs. Note that the smaller the FOM the better. There is a need for structures that provide an improved figure of merit.

There is a drive to reduce the dimensions of trench MOSFETs, as for transistors generally. In the context of the devices considered here, the main benefit of this is to reduce the active area and so reduce $R_{ds,on}$. Such reduced size trench MOSFETs can be made, for example, using deep ultra-violet lithography.

However, this reduction in size is not necessarily attractive for the control FET since in a conventional structure the gate drain charge density Q_{gd} increases drastically with reduced size. Thus, simply reducing the size of the structure does not give improvements as large as might be expected.

There is thus a need for an improved structure to give improved properties of FETs for VRMs.

According to the invention there is provided an insulated gate field effect transistor including: a source region of first conductivity type; a body region of second conductivity type opposite to the first conductivity type adjacent to the source region; a drift region of exclusively the first conductivity type adjacent to the body region; a drain region of first conductivity type adjacent to the drift region, so that body and drift regions are arranged between the source and drain regions, the drain region being of higher doping density than the drift region; and insulated trenches extending from the source region through the body region and into the drift region, each trench having sidewalls, and including insulator on the sidewalls, and a conductive gate electrode, wherein the base of each trench is filled with an insulator plug adjacent to substantially all of the length of the drift region between the body region and the drain region, and the respective gate electrode is provided in the trench over the plug adjacent to the source and body regions.

The invention uses the reduced surface field (RESURF) effect but unlike conventional RESURF transistors the RESURF is non-optimal in that the trench adjacent the drift region is filled with insulator, not gate electrode. Further, unlike some devices in which the drift region has stripes of both conductivity types to obtain a significant reduced surface field (RESURF) effect, the invention uses a drift region of single conductivity type.

In spite of the highly non-optimal RESURF effect achieved in the present invention the device can nevertheless achieve a reduced $R_{ds,on}$ for the same breakdown voltage compared with conventional trench MOSFETs. The drift doping concentration may be raised compared to a conventional FET, which can contribute to Q_{gd} but this may be compensated for by the thick dielectric between gate and drain.

The device achieves this result in a way that is much simpler to manufacture than devices using doping of both n- and p-type in the drift region.

The plug may be a dielectric filler filling the trench between the insulator on the sidewalls adjacent to the drain. Alternatively, the plug may fill the entire

base of the trench, and sidewall insulator provided only above the plug to insulate the gate electrode from the body and source regions.

Preferably, the doping concentration in the drift region is non-uniform, further preferably linearly graded, and preferably the doping concentration is higher adjacent to the drain region than adjacent to the body region. The Q_{gd} value is determined to a significant extent by the depletion charge and this is addressed using the graded doping profile, which achieves an improvement in Q_{gd}.

Calculations (presented below) show that the invention can achieve a significant improvement in the $R_{ds,on}$ value with some improvement in Q_{gd}. Thus, the figure of merit of the device according to the invention is improved signifcantly over prior art devices.

In embodiments, the body doping concentration is in the range 0.5 to 3x 10^{17} cm^{-3}, and the drift doping concentration is in the range 10^{15} to $2x10^{17}$ cm^{-3}. Specific values may be selected to provide an appropriate trade-off between $R_{ds.on}$ and Q_{gd}.

The invention is of particular application to a vertical trench MOSFET, i.e. a MOSFET having a semiconductor body having opposed first and second major surfaces, wherein the source region is at the first major surface over the body region, the body region is over the drift region and the drift region is over the drain region, and the trench extends from the first major surface towards the second major surface through the source, body and drift regions.

Note that in this specification the term "over" is used for the direction towards the first major surface and "under" for the direction towards the second major surface without any orientation in space of the MOSFET being intended.

In particular, the transistor may have a plurality of cells, each cell having a source region at the centre of the cell surrounded by the insulated trench.

The cells may have a hexagonal geometry, or a rotated square geometry.

Alternatively, the cells may be stripes arranged laterally across the first major surface with alternating sources and trenches.

The cell pitch may typically be in the range 0.2 to 0.7 micron, for breakdown voltages up to 30V. For higher breakdown voltages, the trench may be deeper than otherwise, and this can lead to a requirement for an increased cell pitch, for example up to 1.5 microns or even higher for higher breakdown voltages still.

The trench may have gate oxide on the sidewalls and the base of the trench adjacent to the drift region may be filled with filler oxide between the gate oxide on the sidewalls. Alternatively, nitride or oxynitride can be used as the filler.

Embodiments of the invention will now be described, purely by way of example, with reference to the accompanying drawings in which:

Figure 1 shows a cross-sectional side view of a MOSFET according to a first embodiment of the invention;

Figure 2 shows a top view of the embodiment of Figure 1;

Figure 3 shows the doping profile of a MOSFET according to the first embodiment; and

Figure 4 shows the top view of a MOSFET according to a second embodiment of the invention.

Note that the drawings are schematic and not to scale. Like reference numerals are used for the same or similar features in different figures.

Figure 1 shows a cross-section through a semiconductor device according to a first embodiment of the invention. A silicon semiconductor body 2 has opposed first 4 and second 6 major surfaces. An n+ drain region 8 adjoins the second major surface. An n- drift region 10 is provided on top of the drain region 8, a p body region 12 on top of the drain and an n+ source region 14 on top of the body region 12. A source contact 16 is provided on the first major surface 4 to connect to the source region 14 and a drain contact 18 is provided on the second major surface 6 to connect to the drain region.

A trench 20 extends from the first major surface 4 through the source region 14, the body region 12 and the drift region 10, having sidewalls 22 and

a base 24 close to the drain region-drift region interface 26. Gate oxide 28 is provided on the sidewalls 22. The base of the trench 20 is filled with oxide dielectric filler 30 adjacent to the drift region 10. Above the dielectric filler 30 is provided a polysilicon gate 32 adjacent to the source region 14 and body region 12. A gate contact 38 connects to the gate 32.

As illustrated in Figure 2, in the specific example, a plurality of cells 40 extend across the first major surface to define a plurality of stripes in which the source region 14 and trench 20 alternate. The cell pitch is 0.5 micron, and the trench is 1.2 microns deep and 0.25 micron wide. Line A-A indicates where the section of Figure 1 is taken. As the skilled person will appreciate, these size values can be changed as required.

The p-type body region 12 extends to a depth of 0.6 micron, and is exposed at the first major surface 4 so that it can be connected to the source contact 16 at a location spaced away from line A-A. For clarity, the source contact 16 is not shown in Figure 2.

The doping profile is shown as a function of depth in Figure 3. The drift region 10 doping concentration varies from $5x10^{15}$ cm^{-3} at the junction of the body 12 and drift region 10 and increases linearly to a value of approximately 10^{17} cm^{-3} at the drift-drain interface 26. The drain region is doped 10^{19} cm^{-3} n-type, the body region 10^{17} cm^{-3} p-type and the source is heavily doped 10^{21} cm^{-3} n -type.

In this specific example the breakdown voltage BV has been calculated to be 25V, with the breakdown occurring near the p-body region 12/drift region 10 junction. A value of $R_{ds,on}$ of 1.1 $m\Omega.mm^2$ excluding the substrate resistance has been calculated for a gate-source voltage of 10V and Q_{gd} has been calculated to be 2.2nC/mm^2 for a drain-source voltage of 12V. This gives a figure of merit of 2.4 mΩ.nC. This compares to 6.3 mΩ.nC for a conventional trench MOSFET with a 200nm thick trench base oxide, the same pitch, trench width and breakdown voltage as the example but with a constant drift doping density.

The invention can thus give very significantly improved figures of merit.

In a second embodiment, instead of a stripe geometry a cell geometry is used, as shown in Figure 4 which shows a hexagonal geometry. The centre of each hexagonal cell includes the stack of source 14, body 12 and drift 10 regions, and an interconnecting matrix of trenched gates 32 surrounds the cells.

Calculations have been carried out and give a value of $R_{ds,on}$ of 1.4 $m\Omega.mm^2$ excluding the substrate resistance for a gate-source voltage of 10V and a Q_{gd} of 1.6nC/mm^2 for a drain-source voltage of 12V. This gives a figure of merit of 2.2 $m\Omega.nC$. This is even better than the embodiment of Figure 1. The p-type body 12 doping density may be increased slightly if a higher threshold voltage is required. Alternatively, p-type instead of n-type polysilicon can be used for the gate conductive layer which also increases the threshold voltage.

The figure of merit of a recently published LDMOS structure (Ludikhuize A W, ISPSD p 301-304, 2002) is 22 $m\Omega.nC$. This is for a larger cell size but even scaling to a 0.5 micron pitch still gives rise to a Q_{gd} of 6.6 nC/mm^2. Thus the invention provides much better results than this published value.

From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications may involve equivalent and other features which are already known in the design, manufacture and use of semiconductor devices and which may be used in addition to or instead of features described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of disclosure also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to any such features and/or combinations of such features during the prosecution of the present application or of any further applications derived therefrom.

For example, the p-type and n-type layers may be reversed.

Instead of a silicon body, the invention may also use other semiconductor materials, including for example III-V materials.

For example, the oxide dielectric in the trench can be replaced with nitride or oxynitride. This should increase Q_{gd} but decrease $R_{ds,on}$. A low-k material may be used which should have the opposite effect.

Instead of a polysilicon gate other materials can be used. In particular, a silicide gate can be used.

Also, although the specific embodiment uses separate gate oxide and trench filler it is also possible to implement the invention using a single dielectric in the trench.

A 1 of n principle may be used. In this arrangement, an additional source field plate may be provided in 1 out of every n trenches.

The invention may also be applied in lateral trench MOSFETs.

CLAIMS

1. An insulated gate field effect transistor, comprising:

a source region (14) of first conductivity type;

a body region (12) of second conductivity type opposite to the first conductivity type adjacent to the source region;

a drift region (10) of exclusively the first conductivity type adjacent to the body region;

a drain region (8) of first conductivity type adjacent to the drift region, so that body and drift regions are arranged between the source and drain regions, the drain region being of higher doping density than the drift region; and

insulated trenches (20) extending from the source region (14) through the body region (12) and into the drift region (10), each trench (20) having sidewalls (22), and including insulator (28) on the sidewalls, and a conductive gate electrode (32) between the insulating sidewall,

wherein the base of each trench (20) is filled with an insulator plug (30) adjacent to substantially all of the length of the drift region (10) between the body region (12) and drain region (8), and the respective gate electrode (32) is provided in the trench (20) over the plug (30) adjacent to the source and body regions (14,12).

2. An insulated gate field effect transistor according to claim 1 wherein the doping concentration in the drift region (10) is lower adjacent to the body region than adjacent to the drain region.

3. An insulated gate field effect transistor according to any preceding claim wherein the doping concentration in the body region (12) is in the range 0.5 to 3x 10^{17} cm^{-3}, and the doping concentration in the drift region (10) is in the range 10^{15} to 2x10^{17} cm^{-3}.

4. An insulated gate field effect transistor according to any preceding claim wherein the plug (30) is of dielectric filler filling the trench

between the insulator (28) on the sidewalls (22) adjacent to the drain region (10).

5. An insulated gate field effect transistor according to any preceding claim having a semiconductor body (2) having opposed first (4) and second major surfaces (6),

wherein the source region (14) is at the first major surface over the body region (12), the body region (12) is over the drift region (10) and the drift region (10) is over the drain region (8), and

the trench extends from the first major surface towards the second major surface through the source (14), body (12) and drift (10) regions.

6. An insulated gate field effect transistor according to claim 5 having a plurality of cells (40), each cell having a source region (16) at the centre of the cell surrounded by the insulated trench (20).

7. An insulated gate field effect transistor according to claim 6 wherein the cells (40) have a hexagonal geometry.

8. An insulated gate field effect transistor according to claim 6 or 7 wherein the trench (20) has gate oxide (28) on the sidewalls, and the base (24) of the trench adjacent to the drift region (10) is filled with filler oxide (30) between the gate oxide (24) on the sidewalls (22) on either side of the trench.

9. An insulated gate field effect transistor according to claim 5 having a plurality of cells (40), arranged as stripes across the first major surface (4) with alternating trenches (20) and source regions (14).

10. An insulated gate field effect transistor according to any of claims 6 to 10 wherein the cell pitch is in the range 0.2 to 0.7 micron.

ABSTRACT

TRENCH MOSFET

The invention relates to a trench MOSFET with drain (8), drift region (10) body (12) and source (14). In order to improve the figure of merit for use of the MOSFET as control and sync FETs, the trench (20) is partially filled with dielectric (24) adjacent to the drift region (10) and a graded doping profile is used in the drift region (10).

[Fig. 1]

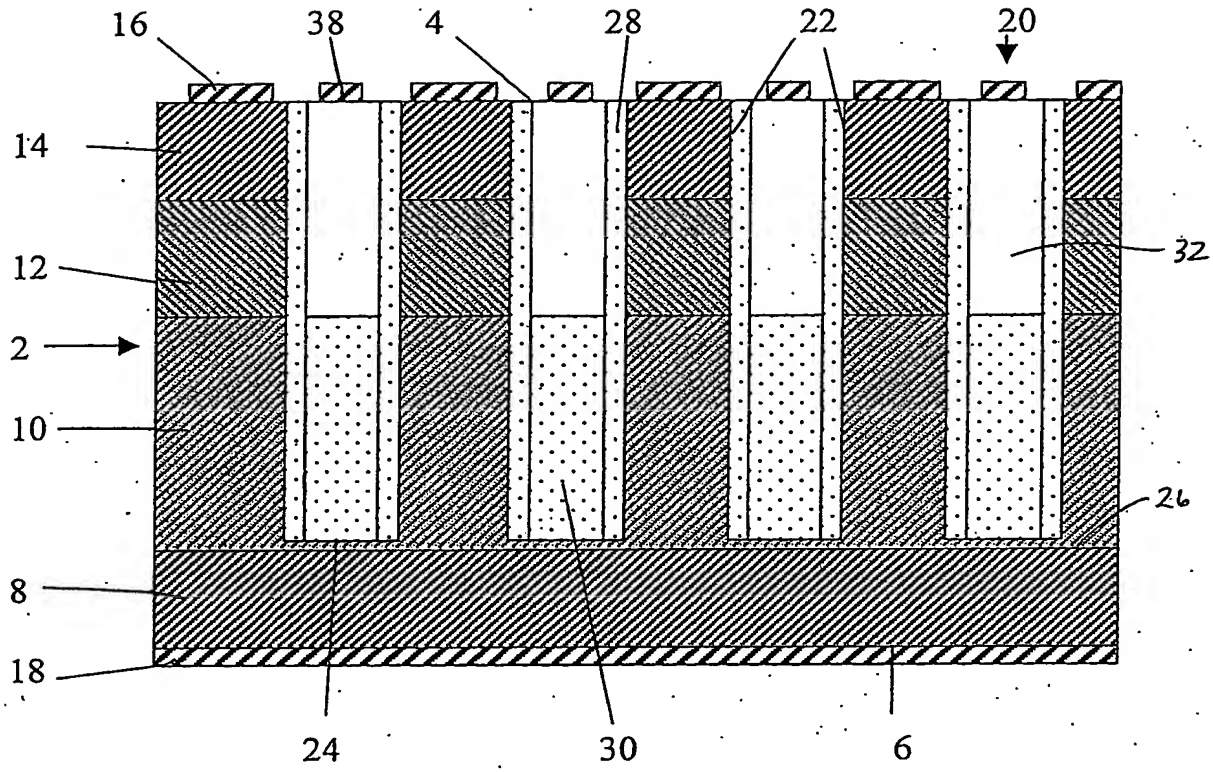

Fig. 1

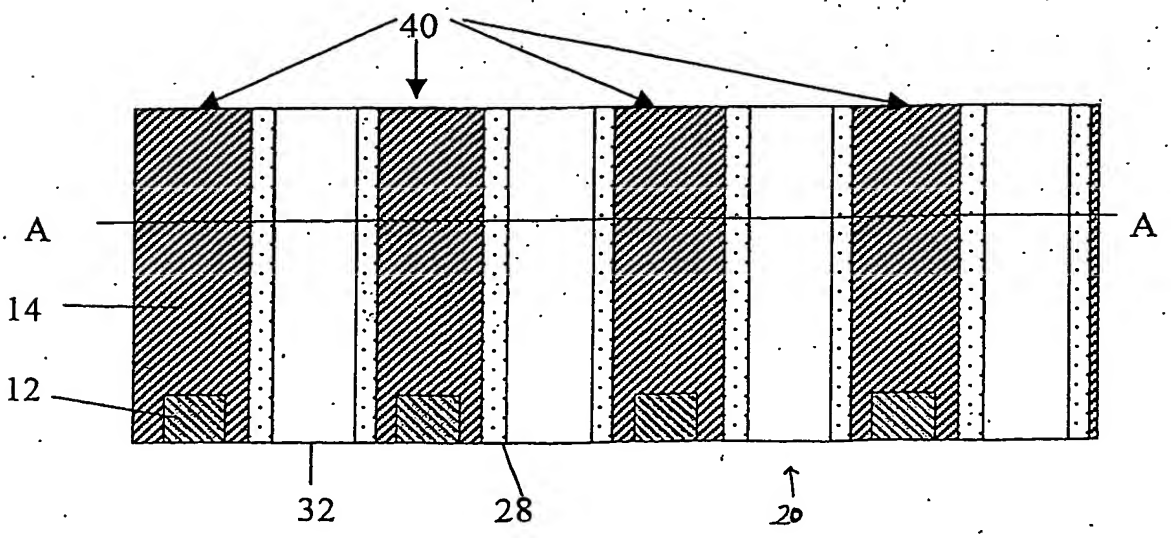

Fig. 2

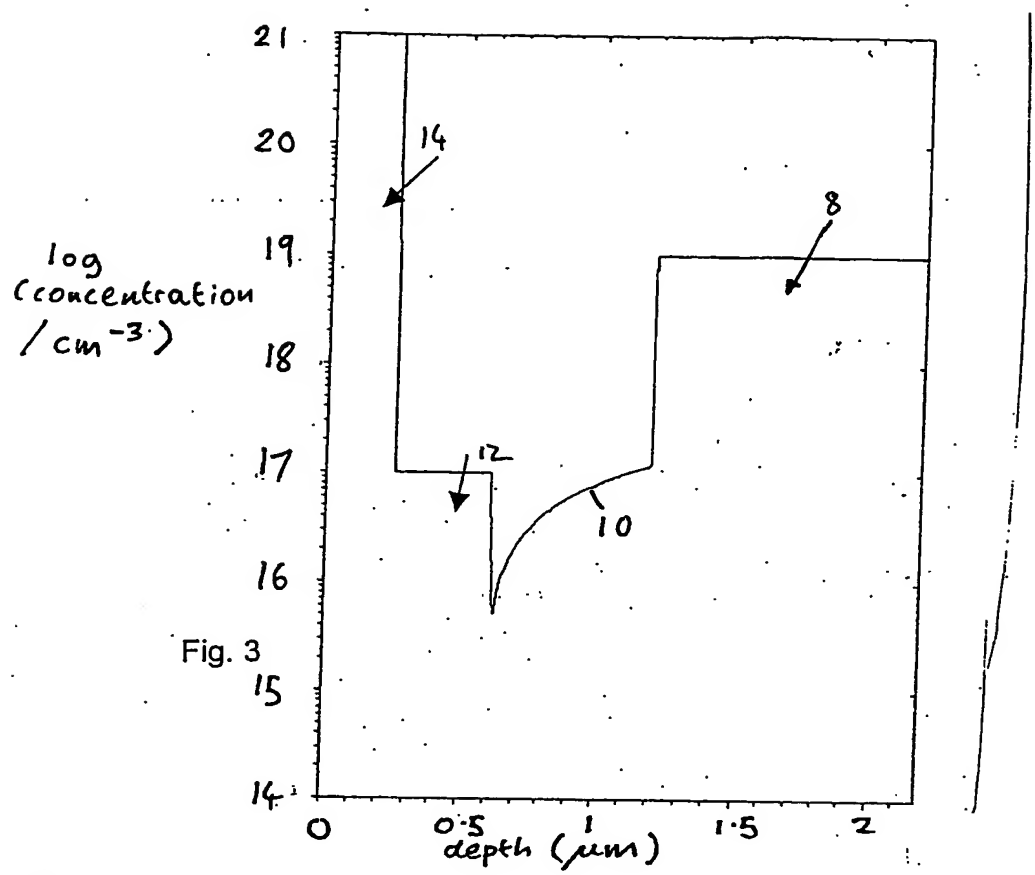
21
20
19
18
17
16
15
14
log (concentration /cm^{-3})
14
8
12
10
0
0·5
1
1·5
2
depth (μm)

Fig. 3

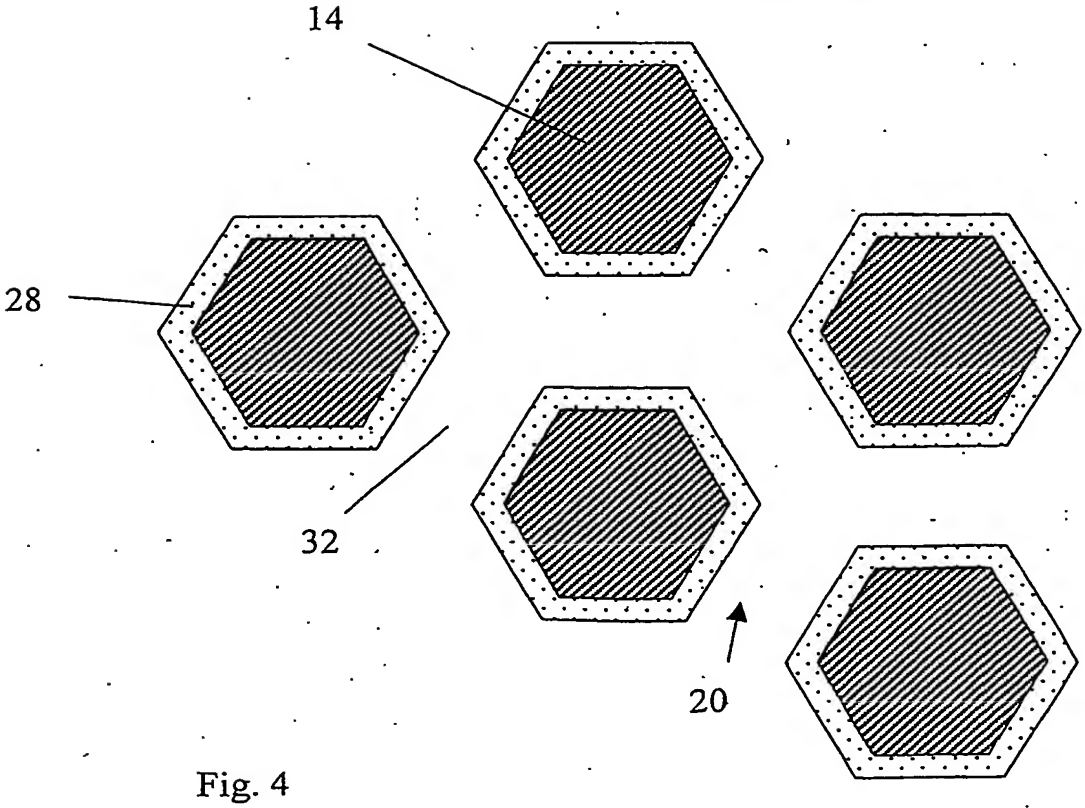
14
28
32
20

Fig. 4